Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Previously Presented) A wiring substrate, comprising:

a wiring layer formed on a substrate; and

terminal electrodes that are coupled to the wiring layer and disposed on the substrate in a manner to avoid diagonal lines thereof.

3. (Previously Presented) A wiring substrate, comprising:

a wiring layer formed on a substrate;

terminal electrodes that are coupled to the wiring layer and disposed on the substrate; and

stress insulation sections provided along diagonal lines of the substrate.

4. (Previously Presented) The wiring substrate according to claim 3, the stress insulation sections being at least one of grooves and slits.

5. (Previously Presented) A wiring substrate, comprising:

a wiring layer formed on a substrate;

terminal electrodes that are coupled to the wiring layer and disposed on the substrate; and

dummy terminals that are provided in four corners or on diagonal lines of the substrate.

6. (Previously Presented) A semiconductor device, comprising:

a semiconductor chip having an active region and pad electrodes formed thereon;

a stress buffer layer formed on the active region;

bump electrodes that are formed on the stress buffer layer and disposed based on a stress distribution that works on the semiconductor chip;

rearrangement wiring layers that couple the bump electrodes and the pad electrodes; and

a protection layer that is formed over the rearrangement wiring layers and the pad electrodes.

7. (Previously Presented) A semiconductor device, comprising:

a semiconductor chip having an active region and pad electrodes formed thereon;

a stress buffer layer formed on the active region;

bump electrodes that are formed on the stress buffer layer and disposed in a manner to avoid diagonal lines thereof;

rearrangement wiring layers that couple the bump electrodes and the pad electrodes; and

a protection layer that is formed over the rearrangement wiring layers and the pad electrodes.

8. (Previously Presented) A semiconductor device, comprising:

a semiconductor chip having an active region and pad electrodes formed thereon;

stress buffer layers that are formed on the active region, and divided and disposed along diagonal lines;

bump electrodes formed on the stress buffer layers;

rearrangement wiring layers that couple the bump electrodes and the pad electrodes; and

protection layers that are formed over the rearrangement wiring layers and the pad electrodes, and divided and disposed along the diagonal lines.

9. (Previously Presented) A semiconductor device, comprising:

a semiconductor chip having an active region and pad electrodes formed thereon;

a stress buffer layer that is formed on the active region;

bump electrodes formed on the stress buffer layer;

dummy bumps provided in four corners or on diagonal lines of the stress buffer layer;

rearrangement wiring layers that couple the bump electrodes and the pad electrodes; and

a protection layer that is formed over the rearrangement wiring layers and the pad electrodes.

10. (Previously Presented) A semiconductor module, comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are coupled to the wiring layer and disposed based on a stress distribution that works on the interposer substrate; and

through hole wirings that are provided in the interposer substrate and couple the semiconductor chip and the wiring layer.

11. (Previously Presented) A semiconductor module, comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are coupled to the wiring layer and disposed on the back surface of the interposer substrate in a manner to avoid diagonal lines; and

through hole wirings that are provided in the interposer substrate and couple the semiconductor chip and the wiring layer.

12. (Previously Presented) A semiconductor module, comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are coupled to the wiring layer and disposed on the back surface of the interposer substrate in a manner to avoid diagonal lines;

at least one of grooves and slits provided along diagonal lines of the interposer substrate; and

through hole wirings that are provided in the interposer substrate and couple the semiconductor chip and the wiring layer.

13. (Previously Presented) A semiconductor module, comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are coupled to the wiring layer and disposed on the back surface of the interposer substrate;

dummy bumps provided in four corners or on diagonal lines of the back surface of the interposer substrate; and

through hole wirings that are provided in the interposer substrate and couple the semiconductor chip and the wiring layer.

14. (Previously Presented) An electronic device, comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are coupled to the wiring layer and disposed on the back surface of the interposer substrate in a manner to avoid diagonal lines;

through hole wirings that are provided in the interposer substrate and couple the semiconductor chip and the wiring layer;

a mother substrate having the interposer substrate mounted thereon; and

an electronic component that is coupled to the bump electrodes through the mother substrate.

15-22. (Canceled)